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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/476,622 | 12/31/1999 | Howard Chin | 884.101US1 | 8079 |

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| EXAMINER | |
|---|---|
| TREAT, WILLIAM M | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | |

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/476,622 | CHIN ET AL. | |
| | Examiner | Art Unit | |
| | William M. Treat | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *21 and 29-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21 and 29-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 21 and 29-40 are presented for examination.

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 21 and 29-40 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

4. Claim 21 recites "said processor to execute an instruction that updates microcode" (lines 5-6). Claim 29 recites "executing an instruction to update the microcode" (line 8). Claim 35 recites "an instruction that, when executed by a processor, updates microcode" (lines 4-5). Claim 38 recites "an instruction that, when executed by a processor, updates microcode". Rosenberg's Dictionary of Computers, Information Processing & Telecommunications defines microcode as "one or more microinstructions". He defines microinstruction as "an instruction of a microprogram" or "a basic or elementary machine instruction". Nowhere, in applicants' original disclosure can the examiner find any "instruction to update microcode". There is support for an instruction which modifies a bit of a machine specific register. There is also support for the value of that bit affecting the behavior of a functional unit/logic unit. But, as stated earlier, applicants' original disclosure does not support a claim to an "instruction to update microcode" and, more specifically, does not support an "instruction which

modifies microcode" while at the same time modifying bits in a machine specific register. Therefore the new matter should be cancelled from the claims.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 21 and 29-40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. See paragraph 4, *supra*.

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 21, 29-34, and 38-40 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Dao et al. (Patent No. 4,923,223).

9. First, it is highly relevant that in the course of the prosecution of this application that applicant has set forth the definition that he wishes applied to the term, "machine specific register(s)," when it lacks additional claim language to further define it. On the fifth page of the document filed on 1/24/2003 entitled "Supplemental Response to Summary Office Action Under 37 CFR 1.111", applicant argued "the term 'machine specific register' has been defined as a synonym for registers associated with processor functional units in the original Application." The argument was again repeated in papers filed on 2/21/2003. The examiner has interpreted applicants' statement to mean that they are seeking to claim a machine specific register is any register which may be

accessed by one or more of a processor's functional units. Logically, if a functional unit can read and/or write some portion of a register's contents then that register must be associated with that functional unit.

10. Dao taught the invention of exemplary claim 21 including: a system, comprising: a bus (3018, 3012, 3014); a processor (50) including a plurality of machine specific registers (216, 218, 436, 440, 452, 508, 510), wherein each one of the plurality of machine specific registers is associated with one or more functional units (control timing and interface section--52, exponent and sign processor--78, programmable shifter and unpacker--68, and mantissa processor--70) of the processor (50); and a computer readable medium external (3000) to the processor (50) and coupled to the processor (50) by the bus (3018, 3012, 3014), the computer readable medium (3000) to store instructions to implement microcode functions (col. 25, line 49 through col. 26, line 5) which result in changing a value of at least one bit in at least one of the plurality of machine specific registers. Note that, for instance, machine specific registers (436, 440, and 452) are working registers of the mantissa processor (70) which may also be accessed by the programmable shifter and unpacker (68) and that inherently execution of floating point calculations using the floating point microcode (cols. 29-32) would result in changing a value of at least one bit in at least one of the registers.

11. As to claim 29, it differs from rejected claim 21 only in its requirement that a plurality of machine specific registers (for instance, 436, 440, and 452) be associated with at least two functional units (programmable shifter and unpacker--68, and mantissa processor—70) and that one of the two functional units (mantissa processor—70) be

controlled in response to executing the microcode by modifying a value of at least one bit in one of the plurality of machine specific registers (436, 440, and 452). As explained previously, machine specific registers (436, 440, and 452) are working registers of the mantissa processor (70) which may also be accessed by the programmable shifter and unpacker (68) and that inherently execution of floating point calculations using the floating point microcode (cols. 29-32) would result in changing a value of at least one bit in at least one of the registers. As the values in the working registers change, this would affect any subsequent operation(s) of the mantissa processor.

12. As to claim 30, when the programmable shifter and unpacker (68) operates on a value and then writes it to one of registers (436, 440, and 452), it operates to affect the behavior of the mantissa processor (70) as is being claimed. See Figure 3B.

13. As to claim 31, Dao taught the method of claim 29, wherein a logical source register and a logical destination register for executing an instruction of the microcode are selected from the plurality of machine specific registers (col. 31, line 20 through col. 32, line 20). These instructions would inherently use a register to hold the operand which could be accessed by the functional unit doing the conversion (i.e., it would be machine specific based on applicants' arguments and the examiner's interpretation of those arguments) as well as a destination register which could be accessed.

14. As to claim 32, Dao taught the method of claim 29, wherein the at least two functional units (programmable shifter and unpacker--68, and mantissa processor—70) are linked by a communication bus (54, 56, 58, 66, 84) to a data control unit (control

timing and interface section—52) to fetch an instruction of the microcode from the computer readable medium external to a processor(col. 7, lines 1-25 and col. 24, lines 37-41).

15. As to claims 33 and 34, Dao taught the method of claim 29, wherein controlling one of the at least two functional units of the processor in response to executing the microcode further includes: controlling a non-performance critical function, wherein the non-performance critical function is selected from the group consisting of: cache flushing, cache invalidation, setting processor features, reading processor features, machine check handling, floating point calculations, processor diagnosis, architecture handling for backward compatibility, authentication, platform management interrupt, diagnostic functions and debug functions. Dao taught, for instance, floating point calculations (col. 27, line 5 through col. 32, line 25).

16. As to claims 38-40, they differ from rejected claims 21 and 29-34 only in that they require in claim 40 that changing a value of at least one bit in a selected other one of the at least two machine specific registers affects the behavior of the second logic unit. Dao taught this. When the Mantissa Processor (70) modified register 216 and/or 218 which act as inputs to programmable shifter and unpacker (68), this would affect the behavior of the programmable shifter and unpacker.

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

19. Claims 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dao et al. (Patent No. 4,923,223) in view of Yamauchi (Patent No. 5,097,445).

20. As to claim 35, Dao taught storing microcode in firmware external to a processor; executing the microcode by the processor; updating one or more machine specific registers associated with a logic unit on the processor in response to the executing of the programmed code; and controlling one or more functions of the logic unit on the processor based on a value stored in the one or more machine specific registers (see paragraphs 7-14, *supra*). Dao did not teach his processor (50) storing microcode in firmware external to his processor.

21. However, Yamauchi taught the processor storing microcode in firmware external to the processor was old and well-known at the time of applicant's invention (col. 2, lines 29-55 and col. 3, line 43 through col. 6, line 41). He also taught that one of ordinary skill

in the art would be motivated to utilize a rewritable control store so that the control programs can be rewritten when it is necessary to do so (col. 2, lines 38-41).

22. As to claim 36, Dao taught the machine-accessible medium further includes data, which when accessed by the machine, results in the machine performing: moving a value from a general purpose register/(file registers) of the processor (50) to the one or more machine specific registers (AR registers—508 and 510) (col. 31, lines 17-19).

23. As to claim 37, Yamauchi taught the machine-accessible medium further includes data, which when accessed by the machine, results in the machine performing: reprogramming the microcode in the firmware (col. 6, lines 36-41). As to a reason for combination with the teachings of Dao, see paragraph 19, *supra*.

24. The examiner has repeated his earlier rejection though it is unclear what applicants are claiming because of their severe 35 USC 112 problems.

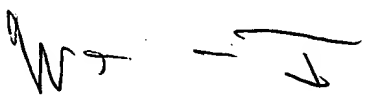
25. Claims 21 and 29-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Margulis (i860 Microprocessor Architecture).

26. As best the examiner can tell because of applicants' rather vague disclosure, applicants and their assignee seem to have borrowed a concept from the i860 microprocessor and claimed it as a new invention without bothering to mention assignee's related art to the examiner. Modifying the RM bits in the floating point status register (pp. 90-92) and having the fix and pfix instructions (p. 140) round based on the value in RM sure sounds exactly like the concept being claimed by applicants though applicants' verbiage obscures the true nature of their claimed invention. The only difference seems to be that the i860 uses a RISC instruction set as opposed to

microinstructions. Anyone of ordinary skill in the art at a company like Intel, IBM, AMD, etc. could readily adapt the concept. One of ordinary skill would be motivated to adapt the concept because it affords flexibility in the instruction set, as when four different modes of rounding are handled by one instruction without modifying that instruction and without having a different instruction for each rounding mode.

27. Any inquiry concerning this communication should be directed to William M. Treat at telephone number (571) 272-4175. The examiner works at home on Wednesdays but may normally be reached on Wednesdays by leaving a voice message using his office phone number. The examiner also works a flexible schedule but may normally be reached in the afternoon and evening on three of the four remaining weekdays.

28. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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